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Investigation on hybrid cascaded multilevel inverter with reduced dc sources

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ABSTRACT

This paper introduces a hybrid cascade multilevel inverter (HCFMLI) topology with bottom standard three-leg and H-bridge cells. The optimal structures of HCMLI are investigated for various objectives, such as minimum number of switches and capacitors, and minimum standing voltage on switches for producing maximum output voltage steps. The suggested topologies introduced herein are most reliable and cost effective when compared with other multilevel based architectures. The operation and performance of the suggested HCMLI's has been verified by the simulation and prototype verifications. Finally, adequate results are presented to confirm the findings.

Contents

1. Introduction

Multilevel converters have received more and more attention because of their capability of high voltage operation (above classic semiconductor limits), high efficiency, and low electromagnetic interference (EMI) [1]. In view of later, different multilevel inverters came into existence. Some of the prominent multilevel based archetypes are Neutral point clamped (NPC), Flying capacitor (FC) and Cascade H-bridge (CHB) multilevel inverter [2]. Fig. 1 articulates the classical and major multilevel topologies However, on comparing the above mentioned structures, CHB stands as a reliable and cost effective archetype because of its functions and features. In recent past, numerous publications are visible on this remarkable topology. However, CHB has a greatest disadvantage, i.e. it uses separate dc source for each H-bridge cell [3]. But, provision of separate dc source for each H-bridge cell, not only increases cost but also effects the reliability.

Indeed, researchers are in hunt of finding solution to above mentioned problem, in fact there is a need of power converter, which uses reduced number of dc sources and semiconductor devices and this paper is devoted for this issue. In this paper we

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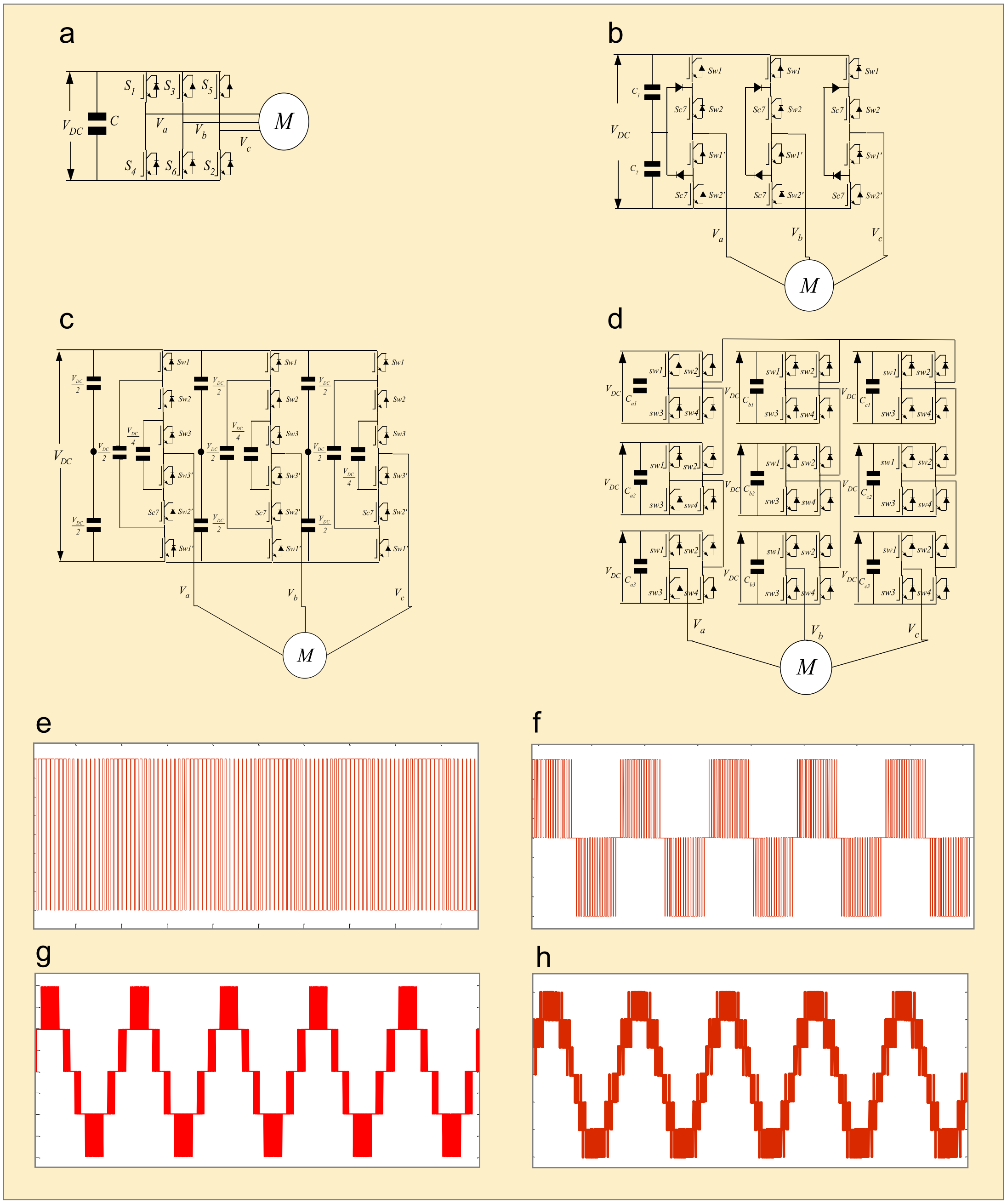

Fig. 1. (a) & (e) Classical inverter and output voltage waveform, (b) & (f) three-Level neutral point clamped output voltage waveform, (c) & (g) five-Level capacitor clamped inverter and output voltage waveform and (d) & (h) seven-Level cascade H-bridge multilevel inverter and output voltage waveform.

investigated two prominent architecture, which uses reduced number of dc sources and switching components. The suggested version in this paper is based on cascade multilevel inverter (CMI). In general CMI's are fabricated by using the same dc source and this is called symmetrical configuration [4]. But if input dc voltages are not the same then it is called asymmetrical configuration. Regarding asymmetrical configuration [5], CMI produces very high quality waveforms, because of its switching states. Although CMI is arranged in asymmetrical fashion they still need separate dc source. To avoid this situation, in this paper we use single dc source for one H-bridge cell and rest of the H-bridge cells are operated with storage devices. In other terms we try to operate with single dc source. This class of arrangement reduces the cost of the equipment. Further, this fabrication need less number of switching components, thus we can improve reliability and reduce the Electromagnetic inference (EMI) problems. However, to verify the suggested versions adequate simulations are carried out with the help of Matlab-Simulink, later it is probed by prototype experiments.

1.1. PWM control strategies of CMI

Together with the advances of multilevel inverter topologies appeared the challenge to extend traditional modulation methods to the multilevel case. On the other hand, there is the inherent extra complexity of having more power electronics devices to control, and on the other the possibility to take advantage of the extra degrees of freedom provided by the additional switching states generated by CMI-topologies [8]. As a consequence, a large number of different modulation algorithms have been developed

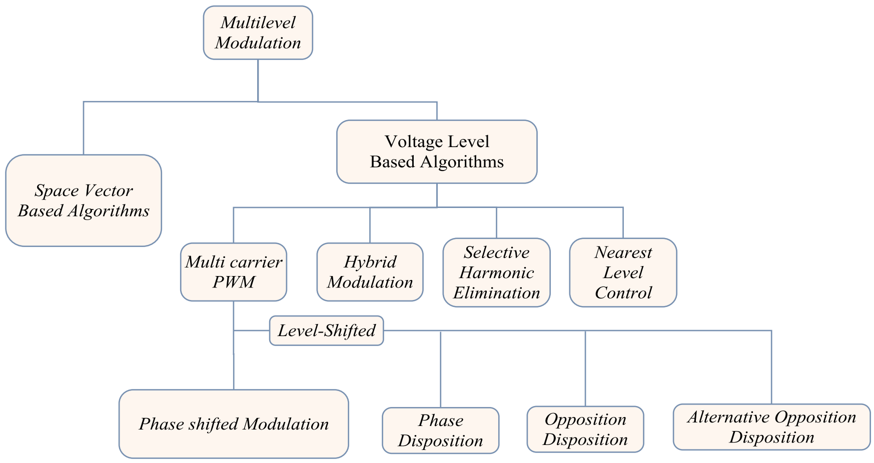

Fig. 2. PWM techniques for CMI based structures.

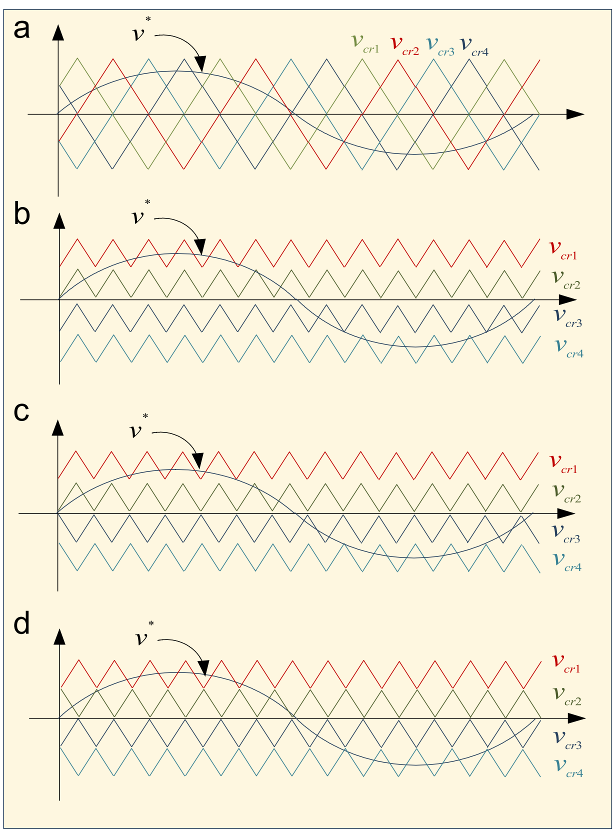

Fig. 3. (a) Phase shifted PWM, (b) phase opposition disposition, (c) opposition disposition and (e) alternative opposition disposition.

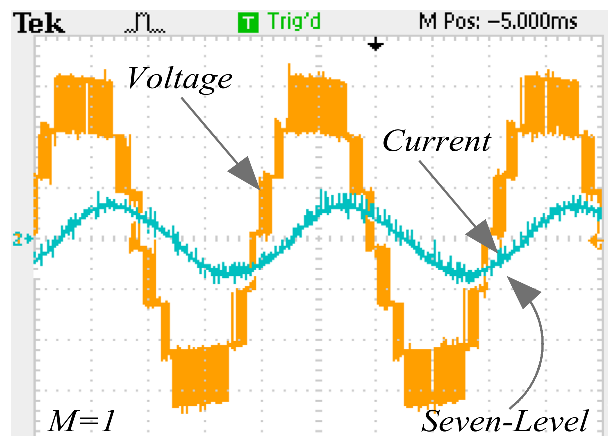

Fig. 4. Details of output voltage (scale: 60 V/div), output current (scale: 6 A/div), time scale: 5 ms/div.

depending on the application and the converter topology, each one having unique advantages and draw-backs [9,10]. A classification of the most common modulation methods for cascade multilevel inverters is presented in Fig. 2. The modulation algorithms are here classified depending on the average switching frequency with which they operate, i.e., high or low. For high-power applications, high switching frequencies are considered, those above 1 kHz. However, HCML are better to operate with PWM switching [11]. As storage elements are involved in the circuit, they need sufficient time to charge and discharge. Regarding PWM methods there are phase shifted and level shifted methods [12]. On comparing both the methods level shifted PWM has gained the capability to produce the qualitative waveforms. So herein, we adopt the level shifted PWM technique.

2. Traditional symmetrical and asymmetrical cascade multilevel inverter

2.1. CMI with equal dc sources

Fig. 1(d) articulates the symmetrical CMI based architecture. These classes of CMIs are introduced in late 1960s. Further, this CMI gained the potential to produce a medium-voltage output based on a series connection of H-bridge cells, which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Due to these merits, the cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market. Further, these archetypes also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation [6]. Therefore, in case of fault condition in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriated switching strategy, it is possible to bypass the faulty module without interrupting the load, bringing an almost continuous overall availability [7,15]. However, to verify this archetype some of the experimental results are presented. Details of prototype setup are presented in subsequent sections. Fig. 4 presents the performance of a seven level CMI with separate dc source. Aforesaid, this is symmetrical configuration, so all the input dc sources are maintain at equal ratios. Due to this fact, output voltage constitutes seven-levels. Further, noteworthy

point is, quality of waveform is quite good and from FFT spectrum (Fig. 5) ***Total Harmonic Distortion*** (THD) is about 12%.

Aforementioned, this is an extremely good architecture, moreover there is no redundancy problems like in NPC converters. Overall, CMI is exceptionally fine. But, separate dc source is a major problem.

2.2. CMI with unequal dc sources

In preceding section, we knew about symmetrical configuration of CMI. Now, Consider Fig. 6 which demonstrates the asymmetrical CMI [13,14,16]. On observing the CMI, input dc source for each H-Bridge cell is arranged with different dc ratios

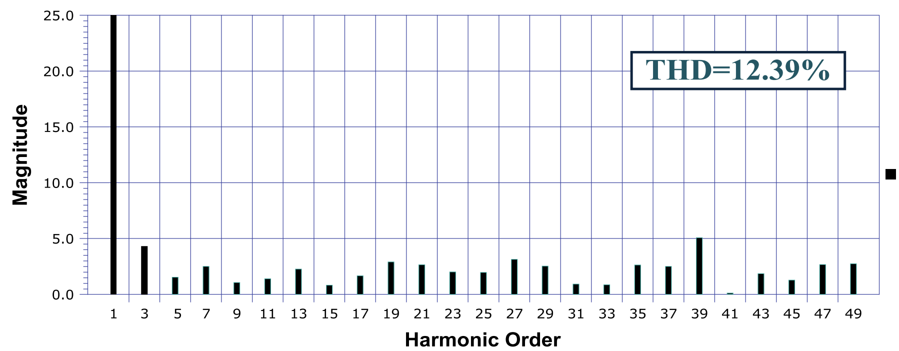

Fig. 5. Cascade multilevel inverter with separate dc source for each H-bridge cell.

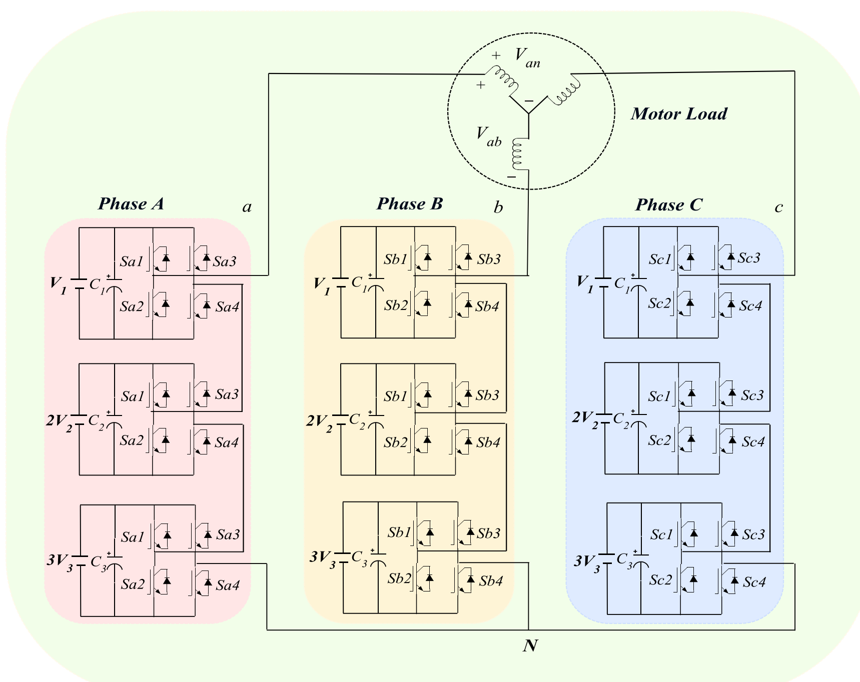

Fig. 6. Cascade multilevel inverter with unequal dc sources.

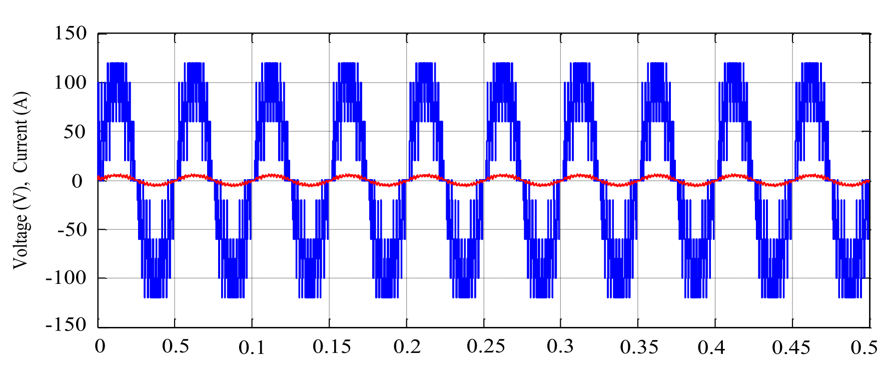

Fig. 7. Simulation verification of asymmetrical CMI.

and the ratios of dc source should be in order like, 1:2:3 or 1:3:9 are in a similar fashion. If not arranged in this fashion, switching states of converter will be complicated and finally there may be short-circuit in the system. For simplicity herein ratios are taken as 1:2:3 for each H-Bridge cells. With this arrangement one can achieve the output voltage waveform with around 13 levels. To confirm this fact, simulation and experimental results are presented in Figs. 7–9. Thus with this criterion we can achieve high quality waveforms. Although we achieve high quality waveforms, but we fail to reduce the dc source count. Moreover at some point we will lose the modularity of architectures. So, it requires adequate care while operating with different dc ratios. In practice these classes of converters are majorly visible in motor drive application. From this section, we can conclude that symmetrical and asymmetrical CMIs are excellent inverters in operating point of view but, large number of dc sources are the only demerit.

To avoid this problem we suggested a CMI with single dc source. Suggested version is demonstrated in the next section.

2.3. Cascade multilevel inverter with hybrid modulation scheme

Figs. 10 and 11 demonstrate the CMI with hybrid modulation scheme and its operation. This class of converters are highly visible in grid connected/Photo voltiac systems. Authors [17] have finite contributions regarding this archtype. Regarding operation point of view, it is quite different while comparing with other swtiching approaches. In this switching synthesis, one converter is operated in mode PWM bridge and rest in fundemntal switching mode. This helps to nullify the switchig losses and therby increases the efficiency. However, in depth assesment of toplogy can be found in above references.

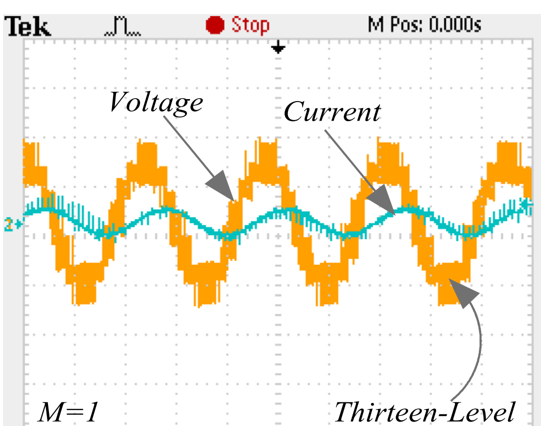

Fig. 8. Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), time scale: 10 ms/div.

In fact there are huge control approaches based on this switching logic. But in all the cases fundemental principle is same. However, for better understanding experimental results and FFT report of output votalge are exposed in Figs. 12 and 13 for CMI with hybrid modulation scheme. Observing keenly, eleven-level output could be predicted in the output votlage wavefrom. At this point readers should observe that, terminal votlages of bridge 2 and 3 are fundamental votlages and terminal votlage for bridge 1 is PWM voltage. Combining all such voltages produces a resultant nine level wavefrom. One of the finest merit is, number of levels in the outptut voltage is drastically increased. But at the same moment its greatest limitation is complexity in switching scheme, and usage of seperate dc sources for each H-Bridge.

3. Hybrid cascade multilevel inverter with single dc source

Further, coming to propose versions, we try to use same concept (which is adopted for Asymmetrical CMI) but we replaced some of the dc sources with energy storage elements. With this

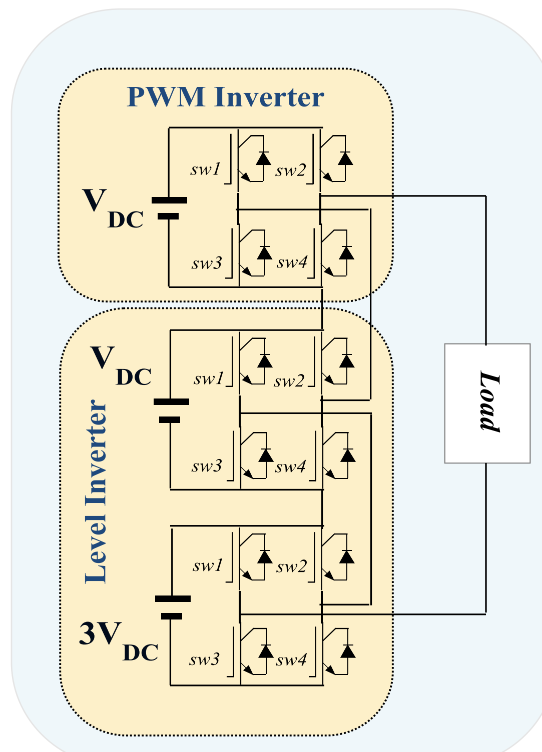

Fig. 10. Cascaded multilevel inverter with hybrid modulation technique.

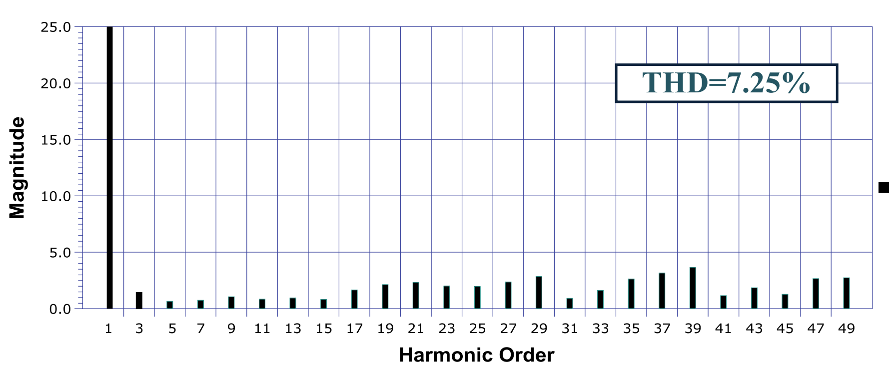

Fig. 9. FFT spectrum for asymmetrical CMI ($m = 1$).

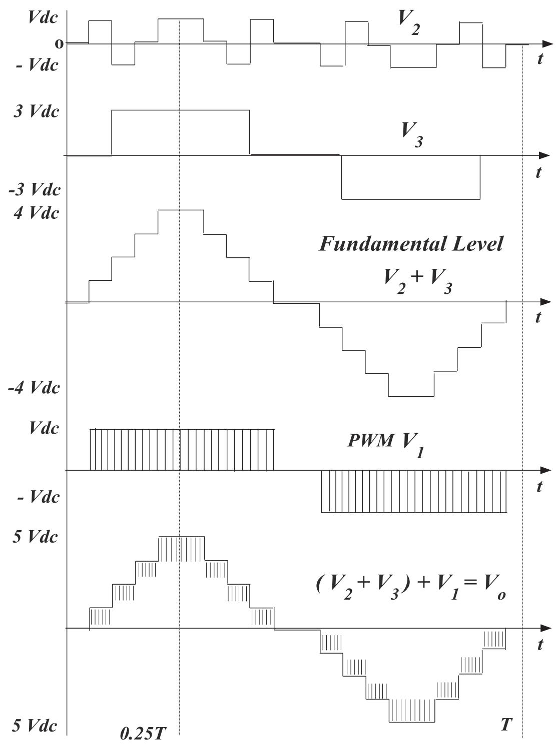

Fig. 11. Output voltage waveforms for cascade H-Bridge multilevel inverter with hybrid modulation scheme.

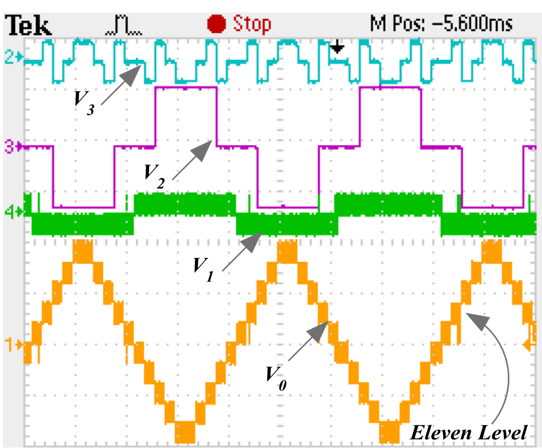

Fig. 12. Experimental output voltage waveforms for cascade H-Bridge multilevel inverter by employing hybrid modulation technique.

arrangement number of dc source will drastically reduce. Moreover cost of equipment considerably diminished. However, to clear this aspect, consider Fig. 14 which demonstrates the hybrid cascade inverter with standard leg and H-bridge inverter. Both inverters operate on same principle but the architectures are different. While on considering Fig. 14 it uses a standard three-leg inverter at the bottom end. This is in fact a strongest arrangement in the inverter design. Because classical inverter is basically a very strong arrangement with great reliability. But only disadvantage is that, they generate low quality waveforms thereby output waveform constitute some amount of lower order harmonics. But on the other hand, they drastically reduce the dc source count.

However, herein, we try to combine the standard inverter with another H-Bridge cell. Thereby we cascade both the inverter and generates a multilevel output. This arrangement is easily extendable. But, for verifications we use only one standard and one H-Bridge cell. Later, one of the important point is, for the entire top H-Bridge cell we used an energy storage element. The principle operation of this archetype is demonstrated in the next section.

Further Fig. 15 represents another HCML with H-bridge cells only. On observing, in place of standard three-leg inverter we replace H-Bridge cell. However, this simply resembles asymmetrical CMI archetype which is demonstrated in previous section. But, one of the major differences is converter operation. Because readers may think that operation is quite same as traditional CMIs, but in converse it is very difficult to stabilize the capacitor voltage. However, for better understanding principle of operation of HCML is demonstrated in the next subsection.

3.1. Principle of operation HCMLI with PWM approach

Topology of HCMLI with three-leg inverter is demonstrated in Fig. 16. Observing keenly, standard leg has a dc power source. The top is an H-bridge cell which is series connected with each bottom three-leg inverter. Further, one of the remarkable points is H-bridge cells utilizes capacitors. Thus topology uses only single dc source. The output voltage v_1 of this leg (with reference to the ground) is either $+V_{dc}/2$ (S5 closed) or $-V_{dc}/2$ (S6 closed). This leg is allied in series with a full H-bridge, which in turn is provided by a capacitor voltage. If the capacitor is utilized and reserved charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S1, S4 closed), 0 (S1, S2 closed or S3, S4 closed), or $-V_{dc}/2$ (S2, S3 closed). Fig. 16 shows an output voltage example. The capacitor's voltage regulation control method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, S5 are closed, depending on whether it is necessary to charge or discharge the capacitor. The method followed here depends on the voltage and

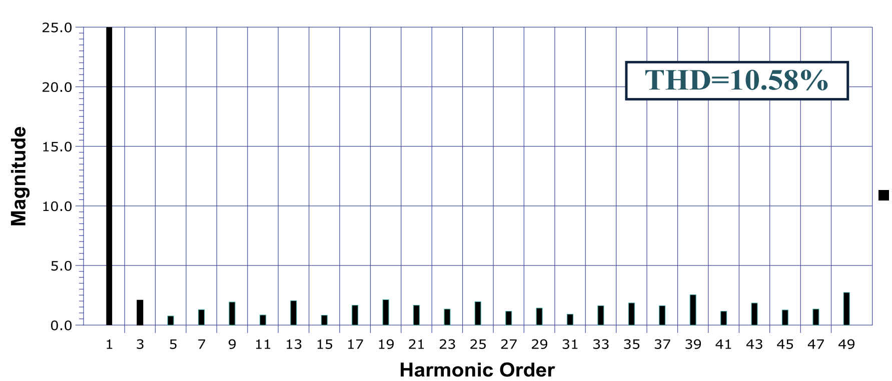

Fig. 13. FFT spectrum for CMI with hybrid modulation scheme.

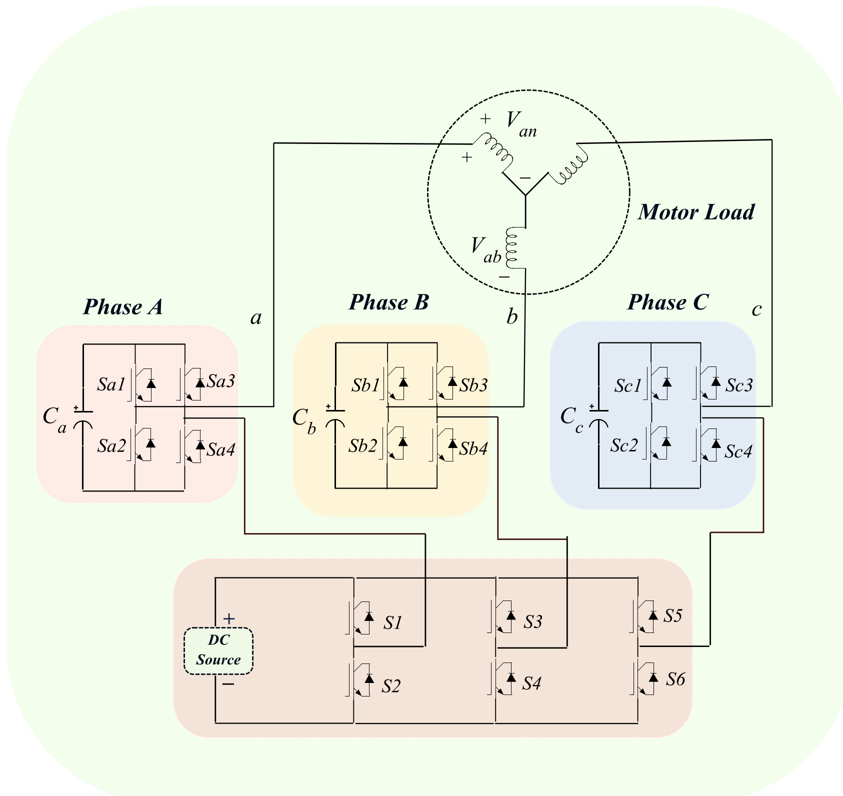

Fig. 14. Hybrid CMI with bottom standard Three-leg inverter.

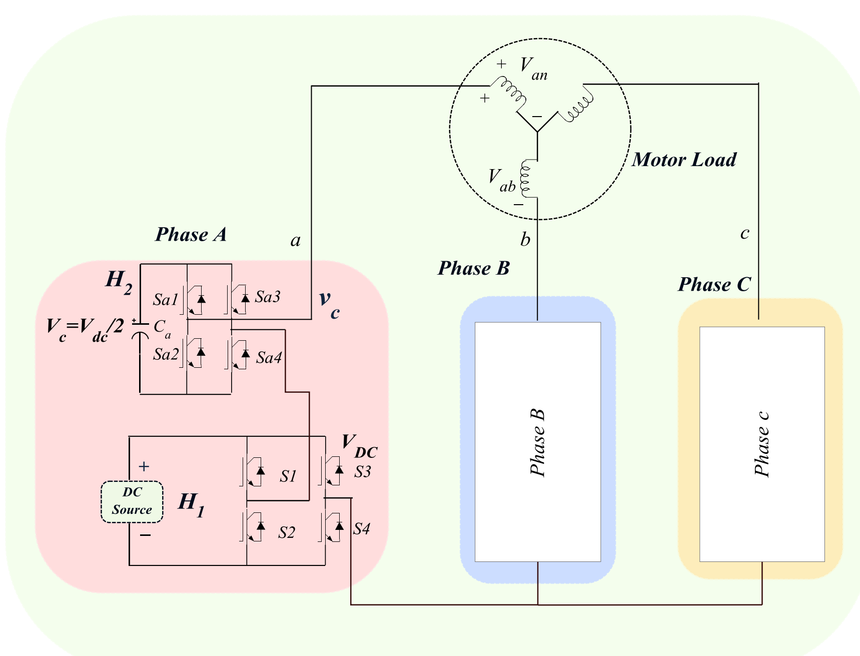

Fig. 15. Hybrid CMI with H-bridge cells.

current not being in phase. It represents that either positive or negative current is needed when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. For suggested HCMLI, level shifted modulation is chosen; details of levels shifted modulation are given in Fig. 3.

In similar fashion, Fig. 17 demonstrates the output characteristics waveforms for *HCMLI* with H-Bridge cells. Aforementioned, this construction utilizes only H-Bridge cells. Further, on observing charging and discharging criterion and output waveform, it appears that, number of steps in the output waveform has been increased. This is because of switching states of converter. To validate this issue, let the dc source for

the first H-bridge (H_1) be a battery or a fuel cell with an output voltage of V_{dc}, while the dc source for the second H-bridge (H_2) be a capacitor whose voltage is to be held at V_c. The output voltage of the first H-bridge is denoted by $v1$ and the output of the second H-bridge is denoted by $v2$. By opening and closing the switches of H1 appropriately, the output voltage $v1$ can be made equal to $-V_{dc}$, 0, or V_{dc}, while similarly the output voltage of H2 can be made equal to $-V_c$, 0, or V_c. Therefore, the output voltage of the inverter can have the values $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, $-V_c$, 0, V_c, $(V_{dc}-V_c)$, V_{dc}, and $(V_{dc}+V_c)$, which constitute nine possible output levels. To balance the capacitor's voltage, not all the possible voltage levels should be used in a cycle. A simple seven-level output voltage case $-3V_{dc}/2$, $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, V_{dc}, $3V_{dc}/2$ can be designed, as shown in Fig. 17, when the capacitor's voltage V_c is chosen as $V_{dc}/2$. By choosing the nominal value of the capacitor voltage to be one-half of that of the dc source, the values of the levels are equal; however, this is not strictly required. The criteria for this capacitor balancing scheme is that: (1) the capacitance value is chosen large enough so that the variation of its voltage around its nominal value is small, generally speaking, one can choose the capacitor–load time constant to be ten times than that of the fundamental period; and (2) the capacitor charging energy is greater than or equal to the capacitor discharge energy in a cycle

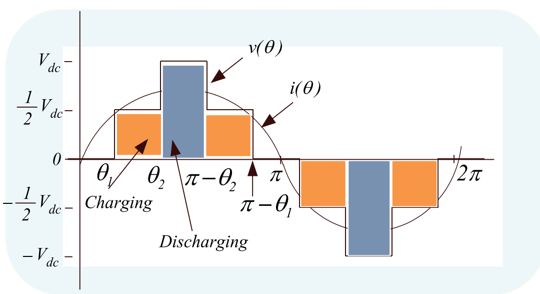

Fig. 16. Key waveforms for charging and discharging of Hybrid CMI with standard inverter.

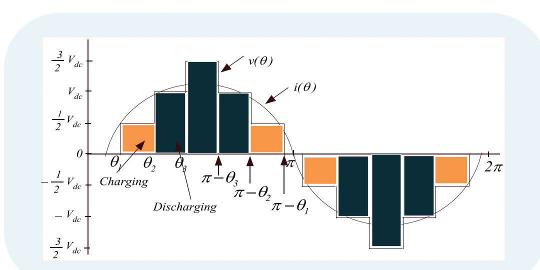

Fig. 17. Key waveforms for charging and discharging of Hybrid CMI with H-bridge inverter.

4. Simulation and experimental results

We performed computer aided simulation and experimental verification to prove the availability of the suggested hybrid multilevel inverter. The simulations are performed through Matlab-Simulink. Regarding experimental verification, a 3 kVA Prototype model of the suggested HCMLI converter is developed and verified in the laboratory. The experiment was carried out for a star connected load. The details of prototype are given in Table 1 and for the experimentation FPGA based module was utilized. An analog expansion daughter board interfaced between the FPGA module and the insulated gate bipolar transistor (IGBT) inverter. Suggested circuit topology and control strategy were realized with code composer. Fig. 18 indicates the construction of hybrid cascaded multilevel inverter. The measured quantities are the load current, load voltages which are measured with hall-effect current and voltage transducers.

Further, Fig. 19 highlights the simulation verification of HCMLI with standard bottom leg inverter. Aforementioned, bottom bridge generates either $+V_{dc}/2$ (S5 closed) or $-V_{dc}/2$ (S6 closed) and this leg is aligned in series with top H-Bridge cells. However, if capacitor is kept charged to $V_{dc}/2$ then resultant output of H-bridge cell would be around $+V_{dc}/2$ (S1 S4 closed), 0 (S1 S2

Fig. 18. Hardware setup for Hybrid CMI inverter.

Table 1

Item				
Type	Switch	Clamping diode	Balancing capacitor	dc-Bus
Diode clamped	$(m-1)\times 2$ 12	$(m-1)\times(m-2)$ 30	NA	$(m-1)$ 18
Flying capacitor	$(m-1)\times 2$ 12	NA	$[(m-1)\times(m-2)]/2$ 15	$(m-1)$ 10
Cascaded FB-cell	$(m-1)\times 2$ 12	NA	NA	$(m-1)/2$ 3
Cascaded FB-cell with hybrid modulation scheme	8	NA	NA	$(m-1)/2$ 3
Suggested HCMLI(with three leg)	10	NA	NA	1
Suggested HCMLI(with H-bridge cells)	8	NA	NA	1

closed) and $-V_{dc}/2$ (S2 S3). Thus summation of bottom and standard leg results to V_{dc} and operation is vice versa for negative V_{dc}. In overall, we can conclude that, output of this arrangement only generates a **Five-Level** voltage waveform. Fig. 16 highlights the experimental results for HCMLI with standard leg inverter. Verification presented in Fig. 20 is taken at modulation index 1. Fig. 21 presents FFT verifications for output waveform. On observing quality of waveform is fine and lower order harmonics are also reduced.

Fig. 22 presents the simulation verification of HCMLI with H-bridge cells only. It is quite clear that, output waveform quality has been improved predominantly. Further, one remarkable point is only bottom H-bride cells are supplied with standard dc sources. Top H-bridge cells are adjusted with capacitors. Operations are similar to previous one; bottom H-bridge voltage generates V_{dc}, where as top H-bridge cell generate V_c ($V_{dc}/2$) which is equal to capacitor charged voltage. On adding both the voltages a seven-level output is retrieved. However, Fig. 23 highlights the experimental results of suggested HCMLI with H-Bridge cells. Verifications are taken at modulation index 1. Fig. 24 presents the corresponding FFT verifications. Observing, quality of wave-form is extremely good. Further lower order harmonics also

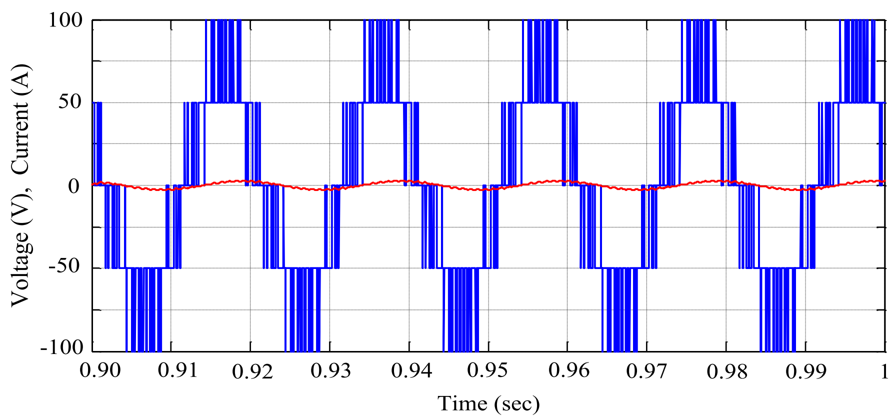

Fig. 19. simulation verification of HCMLI with standard leg inverter.

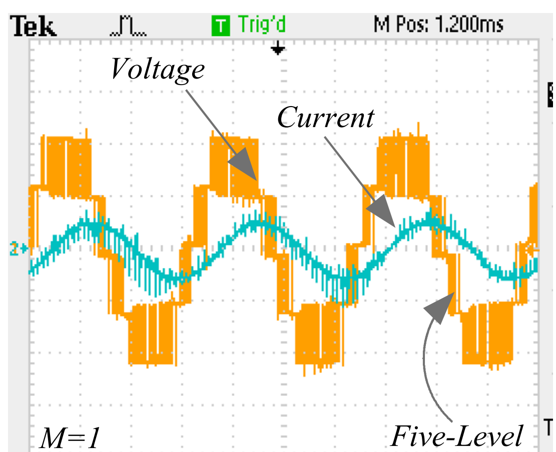

Fig. 20. Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), time scale: 5 ms/div.

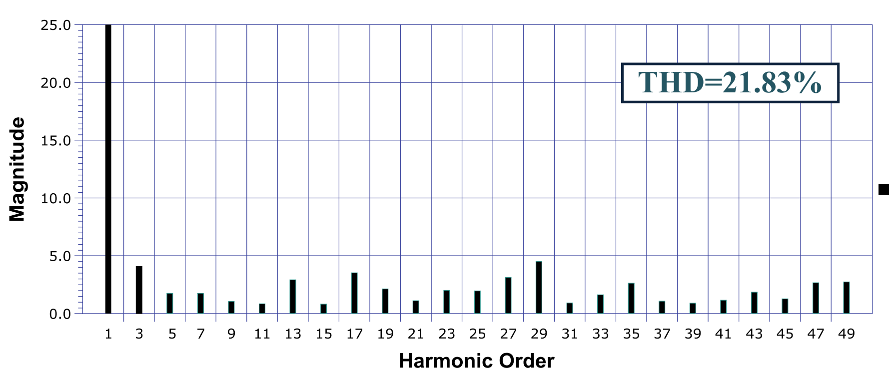

Fig. 21. FFT spectrum for HCMLI with standard leg inverter.

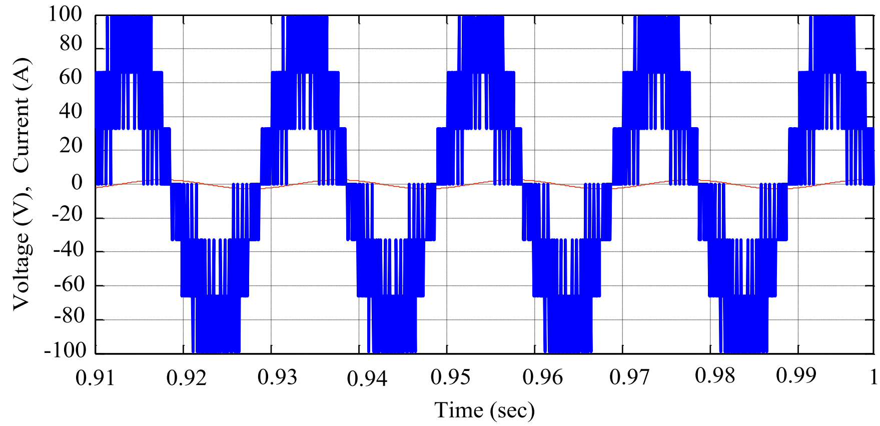

Fig. 22. Simulation verification of HCMLI with H-bridge cells.

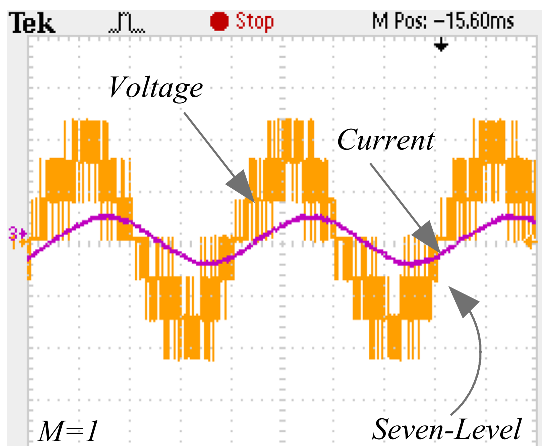

Fig. 23. Details of output voltage (scale: 60 V/div), output current (scale: 6 A/div), time scale: 5 ms/div.

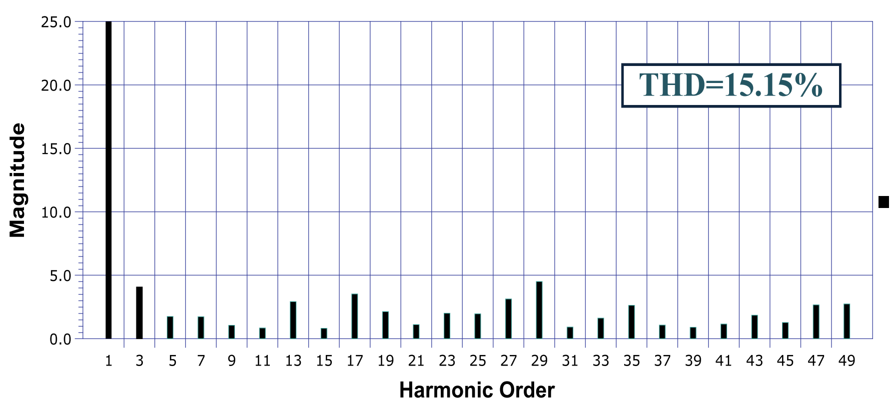

Fig. 24. FFT spectrum for HCMLI with H-bridge cells.

predominately reduced. The main reason behind the quality is **Level Shifted PW**M technique. Thus performances of suggested HCMLI are verified. Later comparative study is done among the traditional multilevel inverters and suggested HCMLI to confirm its merits.

5. Comparative study

To show the merits of suggested architectures a comparative approach is carried out among the traditional multilevel inverters. Table 1 articulates the comparative study, herein comparative approach is done with NPC, FC and CMI based inverter. In general to produce a seven-level phase voltage from an NPC, FC or from a CMI, it requires at least 12 semiconductor switches [17]. Whereas in suggested architectures switching count is 10 and 8. Further, like NPC and FC extra clamping diodes and balancing capacitor are not required. Another remarkable issue is dc-Bus count, in suggested versions only one, whereas in traditional cases it is 18, 10 and 3 for NPC, FC and CMI respectively. Thus form this comparison we can conclude that, suggested version uses less number of switching components to produce same number of output levels.

6. Conclusion

In this paper we suggested a hybrid cascade multilevel inverter based topology. The suggested HCMLIs use only one power source for each phase, while producing desired voltage waveforms. Adding to that, suggested version uses very less number of semiconductor devices when compared to other multilevel based architectures. Thus suggested HCMLI stands reliable and cost effective converters. Moreover as less number of components is used size of equipment drastically comes down. The presented HCMLI based topologies are verified with hardware prototype setup. Adequate results are presented to confirm the findings. In fact with the help of this finding new evolution of technical requirements are fulfilled.

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